CLAIMS

What is claimed is:

1. A laminate for interconnecting an integrated circuit chip, which comprises:

a first layer, wherein the first layer comprises an electrically conducting area and multiple open areas, wherein centroids of two of the open areas define one axis of a Cartesian coordinate system, and wherein the open areas are interspersed inside an outer perimeter of the electrically conducting area;

a second layer, wherein the second layer is electrically insulating, wherein the second layer overlays the first layer; and

a third layer, wherein the third layer comprises multiple electrically conducting traces, wherein the third layer overlays the second layer, wherein at least one of the traces is oriented at other than an orthogonal angle to each axis of the coordinate system, wherein the oriented trace is longer than the spatial extension between two of the open areas, and wherein the projection of the oriented conducting trace onto the first layer lies external to the open areas.

2. The laminate as recited in claim 1, wherein the open areas on the first layer sum to a total open area of at least 10 percent and less than 30 percent of the total area of the first layer.

3. The laminate as recited in claim 1, further comprising:

the integrated circuit, wherein the integrated circuit is attached to the laminate.

4. The laminate as recited in claim 1, further comprising:

a substrate, wherein the laminate is attached to the substrate.

5. The laminate as recited in claim 1, wherein the laminate is mounted in an integrated circuit package.

6. The laminate as recited in claim 1, wherein the laminate is fabricated as part of a printed circuit board.

7. The laminate as recited in claim 1, wherein the second layer material is selected from the group consisting of epoxy resin and teflon.

8. The laminate as recited in claim 1, further comprising:

a fourth layer, wherein the fourth layer is electrically insulating, wherein the first layer overlays the fourth layer; and

a fifth layer, wherein the fifth layer comprises at least one electrically conducting trace, wherein the fourth layer overlays the fifth layer, wherein at least one of the traces is oriented at other than an orthogonal angle to each axis of the coordinate system, wherein the oriented trace is longer than the spatial extension between two of the open areas, and wherein the projection of the oriented conducting trace onto the first layer lies external to the open areas.

9. The laminate as recited in claim 8, wherein the second layer and the

2 fourth layer materials are selected from the group consisting of epoxy resin and teflon.

10. The laminate as recited in claim 1, wherein the open areas have a
2 repeating shape and a repeating size.

11. The laminate as recited in claim 10, wherein the open areas have a
2 repeating orientation with respect to a Cartesian coordinate system.